REMARKS

Status of the Claims

Claims 1-7 and 9-37 are currently pending in the Application. Claims 1, 36, and 37 are independent claims. Claims 1, 2, 36 and 37 have been amended to address informalities and drafting errors noted by the Examiner. No amendments have been made to traverse art cited by the Examiner. Claim 8 has been cancelled. No claims have been added in this Response. Applicants submit that no new matter has been added as a result of any amendments to the claims or specification.

Objection to the Drawings

Applicants note that the Examiner has objected to the drawings under 37 CFR 1.83(a) for failing to show a "machine readable medium" claimed in claim 36. Applicants have amended the drawings and added Figure 9 which shows a "machine readable medium." Support for the newly added drawing is found in the original specification at page 27, lines 1-14, therefore no new matter has been entered. Applicants are sending herewith replacement drawing sheet 2/2 which includes newly added Figure 9.

Objections to the Specification – Informalities

Applicants note that the Examiner has noted various informalities regarding Applicants' specification. First, Applicants note with appreciation that the Examiner identified a drafting error regarding Equation 3. This Equation has been amended in accordance with the suggestion provided by the Examiner.

Second, Applicants note the typographical error noted by the Examiner at page 13, lines 1-4 using the phrase "metallization resistant." This phrase has been amended to read "metallization resistance," as suggested by the Examiner.

Objections to the Specification – Antecedent Basis

Applicants note that the Examiner has objected to the specification as "failing to provide proper antecedent basis for the claimed subject matter." While strict adherence to antecedent basis is required under 35 U.S.C. § 112 for claimed elements, Applicants note that 37 CFR § 1.75(d)(1) provides that "terms and phrases used in the claims must find *clear support* ***or*** *antecedent basis* in the description so that the meaning of the terms in the claims may be ascertainable by reference to the description." (emphasis added). MPEP § 608.01(o) provides, in part, that "The meaning of every term used in any of the claims ***should be apparent from the descriptive portion*** of the specification with clear disclosure as to its import ...." (emphasis added). Applicants further note that Applicants' original claims (i.e., the claims examined by the Examiner in the present Office Action) may be relied upon by the Applicants in establishing Applicants' disclosure (see MPEP § 608.01(l).

Applicants submit that ***clear support*** has been provided for each of the terms objected to by the Examiner. The term "supply voltage" that appears in the original specification has been amended to coincide with the term "power supply voltage" that is included in several of Applicants' originally filed claims. No new matter has been added as a result of this amendment as "power supply voltage" was originally presented in Applicants claims and, furthermore, the original specification used the term "supply voltage (i.e. Vdd)" which provided clear support for the term "power supply voltage" in Applicants' originally filed claims.

The terms "distributed capacitance" and "distributed resistance" were similarly objected to by the Examiner. The terms "metallization resistance and capacitance" are used throughout the specification (see, e.g., page 4, lines 20-25). A shorthand for "metallization resistance and capacitance" is noted as "metallization RC," (page 5, lines 24-25). Applicants note that the shorthand term "metallization RC" is also commonly used for "metallization resistance and capacitance" by those of skill in the art. On page 5, lines 24-25, Applicants note that "metallization RC can also be referred to as internal RC or distributed RC." Based on this description, Applicants respectfully submit that clear support exists in Applicants' disclosure for

any of the terms "internal resistance," "internal capacitance," "distributed resistance," and "distributed capacitance." Applicants submit that no amendments are necessary to address the objection to the use of the terms "distributed resistance," and "distributed capacitance" in Applicants' original claims. However, in order to expedite examination of Applicants' application, Applicants have amended the specification to spell out that the shorthand notation "distributed RC" stands for "distributed resistance," and "distributed capacitance." No new matter has been added as a result of these amendments.

Applicants note that the Examiner has objected to the claimed limitation of "running experiments using the performance model" as not appearing in the specification. Applicants have amended the claims to claim "performing timing analyses" as suggested by the Examiner in the Claim Interpretations section of the Office Action.

Finally, Applicants note that the Examiner objected to the term "transistor impedance." While Applicants disagree that the disclosure does not adequately disclose "transistor impedance," Applicants have separately decided to cancel claim 7. The objection of the term "transistor impedance" is therefore moot.

Claim Objections

Applicants note that the Examiner objected to claims 1, 36, and 37 for informalities related to typographical errors. In addition, the Examiner objected to the preamble of claim 36. Applicants have amended each of these claims addressing the Examiner's objections. Consequently, Applicants respectfully request that the objection of these claims be withdrawn in light of these amendments.

Claim Rejections – 35 U.S.C. § 101

Claims 1-37 stand rejected under 35 U.S.C. § 101 as being directed to non-statutory subject matter. Applicants respectfully traverse the rejections. MPEP §§ 706.03(a) and 2105 – 2107.01 provide rules for rejecting claims as being directed to non-statutory subject matter.

Applicants submit that Applicants claim are clearly statutory and that the Examiner's application of 35 U.S.C. § 101 to Applicants' claims is improper. MPEP § 2106(IV)(B)(2)(b) provides guidance for statutory subject matter of process claims under 35 U.S.C. § 101. This section provides for "safe harbors" of processes when the applicant claims independent physical acts that are performed outside the computer independent of and following the steps to be performed by a computer, whose acts involve the manipulation of tangible physical objects and result in the object having a different physical attribute (MPEP § 2106(IV)(B)(2)(b) citing Diamond v. Diehr, 450 U.S. at 187, 209 U.S.P.Q. at 8). Applicants claims use an algorithm for creating a performance model of a first circuit design, changing the design into a second circuit design, and ***making an integrated circuit*** comprising the second circuit design. Applicants submit that the independent physical act of making the integrated circuit is a safe harbor of statutory subject matter under 35 U.S.C. § 101. Even without this safe harbor, Applicants contend that Applicants' claims are directed to statutory subject matter because they result in physical transformations (i.e. circuit designs) outside the computer and are limited to a practical application within the technological arts, namely circuit design. These statutory requirements are clearly spelled out in MPEP § 2106(IV)(B)(2)(b), first paragraph.

Applicants have traversed the rejections under 35 U.S.C. § 101. Consequently, Applicants respectfully request that the Examiner withdraw the rejections.

Claim Rejections – 35 U.S.C. § 112

35 U.S.C. § 112, First Paragraph – Enablement

The Examiner has rejected ***all*** of Applicants claims (claims 1-37) as being based on a disclosure that is not enabled. Applicants respectfully traverse the rejections. The Examiner rejected claims 1, 36, and 37 as reciting a limitation of an equation which comprises a plurality of variables, one of which is related to transistor performance. The Examiner cites the specification as stating that "the process parameter represents transistor performance fluctuations due to manufacturing process variations" (page 10, lines 23-24). Applicants submit that the

specification is clear and enabling to those of skill in the art. As taught by Applicants in the specification, transistor performance fluctuates based upon the manufacturing process used to create the transistor as well as subtle variations in a particular manufacturing process. These fluctuations are well known to those skilled in the art. Applicants further note that in the background of Applicants' application (pages 1-2), Applicants describe the timing rule currently used in the art today evaluates an equation in the form of:

Equation 1 $$Delay = (K1 + K2 \cdot Cl) \cdot Tx + K3 \cdot Cl^2 + K4 \cdot Cl + K5$$

This prior art equation takes into account the process used to create the transistor. Therefore, it is clear that the "process" parameter is a well known parameter to those skilled in the art and, consequently, Applicants submit that Applicants' claimed invention is enabled to those of skill in the relevant art. (see 35 U.S.C. § 112, MPEP §§ 706.03 and 2164). Applicants further submit that the Examiner failed his burden under the enablement requirement under MPEP § 2164.04. Applicants submit that the Examiner has not construed the claims, as required under MPEP § 2164.04. Instead, the Examiner has called out particular equations and terms used in the specifications without construing Applicants' claims and selecting a definition of the terms that the Examiner intended to use when examining the application.

The above arguments equally apply to the other terms rejected under 35 U.S.C. § 112. Applicants submit that "transistor performance" is known to those of skill in the art in the same way that those of skill in the art have knowledge of a process parameter. Similarly, "transistor process technology" is known to those of skill in the art. As the term clearly implies, and is known to those of skill in the art, it means the technology used to create transistors. Finally, those of skill in the art clearly know how to make an integrated circuit. While "making" an integrated circuit is claimed, the focus of Applicants claimed invention is a circuit resulting from the timing analysis disclosed and claimed by Applicants. Applicants submit that Applicants' claimed invention can be used to "make" an integrated circuit irregardless of the particular methods used to make the circuit. Particular methods used to create integrated circuits are

extremely well known in the art. Applicants have no duty nor obligation under 35 U.S.C. § 112 or the MPEP to teach or regurgitate particular methods used to make integrated circuits when such methods are well known in the art.

Accordingly, Applicants submit that the objections under 35 U.S.C. § 112 – Enablement – have been traversed. In addition, Applicants submit that the Examiner has completely failed to satisfy the examiner's burden in rejecting claims under 35 U.S.C. § 112.

35 U.S.C. § 112, First Paragraph - Best Mode of the Invention

The Examiner has rejected all of Applicants' claims (1-37) under 35 U.S.C. § 112, first paragraph, as failing to disclosed the best mode contemplated by the inventor. Applicants respectfully traverse the rejections. As an initial matter, Applicants are highly offended that the Examiner rejected Applicants' claims as failing to disclose the best mode of Applicants' invention. Best mode rejections are ***"extremely rare"*** during *ex parte* prosecution. MPEP § 2165.03 states as follows (with emphasis added):

> The examiner **should assume** that the best mode is disclosed in the application, unless evidence is presented that is inconsistent with that assumption. It is **extremely rare** that a best mode rejection properly would be made in *ex parte* prosecution. ***The information that is necessary to form the basis for a rejection based on the failure to set forth the best mode is rarely accessible to the examiner***, but is generally uncovered during discovery procedures in interference, litigation, or other *inter partes* proceedings.

The Examiner performs some convoluted mathematical assumptions in rejecting Applicants' claims using a "best mode" rejection because "The influence of the exponential terms on the result, due to the asymptotic behavior of the exponential functions compared to linear functions, will overwhelm the influence of the linear terms." The Examiner further states that "there is not indication that any of the coefficients, once determined, will be non-zero and have literally no influence on the result." (Office Action, para. 22). It simply appears that the Examiner either does not like or does not understand Applicants' equations. The Applicants provide examples of particular exponent values that may be used in Applicants' equations.

Second, simply because, in some circumstances, a "coefficients ... will be non-zero...," is no reason to reject Applicants' claimed invention as failing to disclose Applicants' best mode. It is simply incredulous that the Examiner can state that "it is apparent to the examiner that applicant new of a mode of practicing the invention that the inventor considered to be better than any other." Applicants direct the Examiner's attention to MPEP § 2165.03 which states that (***emphasis in the MPEP***):

> **EXAMINER MUST DETERMINE WHETHER THE INVENTOR KNEW THAT ONE MODE WAS BETTER THAN ANOTHER, AND IF SO, WHETHER THE DISCLOSURE IS ADEQUATE TO ENABLE ONE OF ORDINARY SKILL IN THE ART TO PRACTICE THE BEST MODE**

Applicants submit that the Examiner has completely failed to satisfy the burden required to reject Applicants' claims for failing to disclose the best mode of the invention. Applicants note that the Examiner does not point to the best mode that the Examiner contends that the Applicants have failed to disclose. Instead, the Examiner points to certain characteristics of Applicants' equations and contends that, for some convoluted reasons, the equations show that the Applicants' failed to disclose the best mode of practicing the invention. This simply makes no sense.

Applicants have traversed the rejections and submit that Applicants' disclosure contain the best mode, known to Applicants, of practicing the claimed invention. The Examiner has completely failed to satisfy the burden of establishing a best mode rejection because the Examiner has absolutely no proof that the inventor knew of a mode that was better than the mode that was disclosed. As previously stated, Applicants are highly offended at the Examiner's contention that Applicants failed to disclose the best mode, as known by the Applicants, for practicing Applicants invention. Applicants respectfully insist that the Examiner immediately withdraw this offensive and completely unfounded rejection.

35 U.S.C. § 112, Second Paragraph – Indefiniteness

The Examiner has rejected all of Applicants claims (1-37) under 35 U.S.C. § 112, Second Paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. Applicants respectfully traverse the rejections.

At paragraph 27, the Office Action contends that "it is unclear to the examiner how applicant's [sic] invention can derive a set of constants for the plurality of unknown constants in an equation that comprises a plurality of variables and unknown constants." Applicants submit that page 19 of the disclosure provides ample support and teaches how values for the unknown constants are obtained. Following is an excerpt from Applicants' specification beginning at page 19, line 3:

> In order to collect sufficient data to derive the constants of the equations, at least 21 runs must be performed by a circuit simulator in order to provide sufficient data to solve the 21 unknown equation. That is, at least 21 data points are needed to fully solve the equations. However, these 21 points may be chosen at varying values of metallization resistance and capacitance, Vdd, temperature, process, Tx and Cl in order to provide data for evaluating the equation constants. Therefore, smaller, simpler circuits (as in the case of deriving the exponents) may be used to determine the optimal 21 operating points to use. These points may be chosen such that at least one point focuses on one or more of the critical constant values. For example, the table below illustrates one embodiment of how the constants may be set in order to properly isolate given constants.

To obtain these constants:	**Zero out these processing parameters:**
K5	Tx, Cl, Rint, Cint
K3, K4	Tx, Rint, Cint
K8, K9	Tx, Cl, Rint
K6	Tx, Cint
K7	Tx, Cl
K0, K1	Cl, Rint, Cint
K10	Cl, Rint (also use K0 and K1)
K2	Rint, Cint

Applicants submit that derivation of the constants using Applicants' equations is taught and is quite clear, contrary to the views of the Examiner.

Applicants disagree with the contentions made that claim language found in other claims is generally vague. Claim 5 claims a delay expression that includes a metallization resistance and metallization capacitance delay. As these claimed terms clearly convey, the delay expressions include delay values pertaining to metallization resistance and metallization capacitance. Claims 6-9 are similarly clear and definite regarding the claim elements set forth in these claims.

The terms "metallization resistance and capacitance" are used throughout the specification (see, e.g., page 4, lines 20-25). The claimed term "metallization capacitance delay" obviously means the delay inherent in the metallization capacitance. Likewise, "capacitive load" is described as variable "Cl" in the equations (see page 2, paragraph beginning at line 8). Obviously, "load capacitance delay" means the delay inherent in outputting the capacitive load. Similarly, "process delay" is obviously the delay inherent with the transistor performance (process being defined as transistor performance at page 4, lines 24-25).

Applicants have amended claim 36 to provide antecedent basis for the phrase "the first set of constants" as well as provide that computer program instructions are included in the machine readable medium. Applicants submit that claim 36, as amended, is clear and definite. Accordingly, Applicants respectfully request that the rejection of claim 36 be withdrawn.

Claim Rejections – 35 U.S.C. § 102

Claims 1-3, 36, and 37 stand rejected under 35 U.S.C. § 102 as being anticipated by U.S. Patent No. 5,883,818 to Salimi et al. (hereinafter "Salimi"). Applicants respectfully traverse the rejections.

In independent claim 1, Applicants claim a method for making an integrated circuit that includes the steps of:

- providing a circuit simulator having the capability of simulating changes to at least one of power supply voltage, distributed capacitance, distributed resistance, transistor performance, and temperature;
- providing a first circuit design;
- providing an equation which comprises a plurality of variables and constants, wherein the plurality constants are unknown constants and one of the variables is related to at least one of power supply voltage, distributed capacitance, distributed resistance, transistor performance, and temperature;
- applying the circuit simulator to the first circuit design to derive a first set of constants for the plurality of constants; and
- replacing the unknown constants with the first set of constants to obtain a performance model of the first circuit design;
- performing a first set of timing analyses using the performance model of the first circuit design;
- changing the first circuit design to obtain a second circuit design; and
- making an integrated circuit comprising the second circuit design.

The Office Action contends that Salimi teaches Applicants' claimed method. A review of Salimi shows that Salimi neither teaches nor suggests Applicants' claimed method. Salimi is directed to improving IBM's early timing estimator (ETE). Salimi clearly describes the steps taken to evaluate the operation of an integrated circuit. At col. 1, lines 55 to 67, Salimi describes a process whereby:

1) performance of a logic cell (i.e., circuit design) is evaluated at different operating parameters in order to generate simulation data;
2) a model is generated with at least one modeling function (i.e., equation);
3) the model is generated in order to create modeling data;
4) the modeling data is compared with the simulation data;
5) a determination is made as to whether an error profile is within an acceptable limit based on the comparison; and
6) adding (or deleting) modeling functions until the error profile is within the acceptable limit.

Salimi clearly does not teach or suggest "changing the first circuit design to obtain a second circuit design" as claimed by Applicants. Instead, Salimi is focused on improving the modeling function that corresponds with a given logic cell (circuit). Nowhere does Salimi teach or suggest creating a second logic cell (circuit) based on any of the steps performed by Salimi. Indeed, the stated purpose of the Salimi patent is "to improve the accuracy of the ... equation" (col. 1, lines 38-43).

The Office Action cites various sections of Salimi as teaching the creation of a second circuit design. However, the Office Action's reliance on Salimi, as shown below, is severely misplaced. The Office Action cites Salimi as teaching "changing the first circuit design to obtain a second circuit design" citing col. 3, lines 59-64, col. 5, lines 33-38, and Figure 3, references 220, 230, 240, and 270.

At col. 3, lines 59-64, Salimi teaches:

> If the error profile is not within an acceptable limit, then, in the first iteration of the process, a second modeling function is added to the model and a determination is made whether the error profile was improved by the addition of the second modeling function in step 270.

Here, Salimi is teaching how to increase the accuracy of the model by adding (and sometimes deleting) functions from the model. In the flowchart shown in Figure 3, Salimi shows a loop where additional modeling functions are added to the model and compared with the simulation data to determine whether the error profile of the model is within acceptable limits (Figure 3, steps 220, 230, 250, 260, 280, and 290 and decisions 240 and 270).

Likewise, at col. 5, lines 33-38, Salimi teaches:

> The currently selected set of modeling functions 310, together with the optimized coefficients outputted from coefficient optimizer 370, are used as the model that is exercised in step 220 of FIG. 3, to generate the modeling data compared in step 230.

In the cited section, Salimi is teaching that the model includes a "set of modeling functions" and uses equation coefficients that are output from a coefficient optimizer. The model is used to generate modeling data that is exercised at step 220. The next step of Fig. 3

(step 230) compares the resulting modeling data with the simulation data to determine the error profile. Again, Salimi is teaching improving a model (equations) that describe a circuit so that the error between the model and the simulation is minimized. In other words, Salimi teaches a method of creating a more accurate model that is used to model a circuit design. Important, however, is the fact that nowhere does Salimi teach or suggest creating a new or modified circuit, in sharp contrast to Applicants' claimed invention in both claims 1 and 37 (Applicants' claim 37 including a limitation of "changing the design of at least one of the interconnect, the first design block, and the second design block to obtain a revised path" with the "path" comprising "a first design block, a second design block, and an interconnect coupling the first design block to the second design block").

The Office Action rejects both claims 36 and 37 using "reasons similar to those given for claim 1 above." Therefore, Applicants respectfully assert that the rejections of each of the independent claims has been overcome because Salimi neither teaches nor suggests limitations included in independent claim 1, as described above. Each of the dependent claims rejected under 35 U.S.C. § 102 depend, either directly or indirectly, on claim 1 and, therefore, are allowable over Salimi for at least the same reasons as claim 1 is allowable.

Claim Rejections – 35 U.S.C. § 103

Claims 1-12 stand rejected under 35 U.S.C. § 103 as being obvious and therefore unpatentable over U.S. Patent No. 6,090,152 to Hayes et al. (hereinafter "Hayes") in view of U.S. Patent No. 6,161,211 to Southgate (hereinafter "Southgate". Claims 13-24 stand rejected under § 103 as being unpatentable over Hayes in view of Southgate in further view of U.S. Patent No. 6,507,935 to Aingaran et al. (hereinafter "Aingaran"). Claims 25-35 stand rejected under § 103 as being unpatentable over Hayes in view of Southgate in further view of U.S. Patent No. 5,559,715 to Misheloff (hereinafter "Misheloff"). Applicants respectfully traverse the rejections.

Regarding claim 1, Hayes teaches a system and method for using logical "adders" to account for variations in operating conditions during timing simulations. Hayes specifically ***teaches away*** from using multiplicative derating factors to model voltage and temperature effects on timing performance. Throughout the Hayes reference, Hayes teaches away from using multiplicative derating factors to model performance. In the "Abstract," Hayes unequivocally teaches that "***Rather than using*** the prior art approach of ***multiplicative derating factors to model voltage and temperature effects on timing performance***, adders are used to model the change in performance due to variations in operating conditions (i.e., voltage and temperature)." (emphasis added). In sharp contrast, Applicants claim provides an equation that comprises a number of variables that include multiplicative constants related to voltage and temperature.

Again, in the first sentence of Hayes' detailed description (col. 5, lines 11-14), Hayes teaches that the Hayes reference teaches away from using any multiplicative derating factors in predicting timing delays: "The present invention discloses an alternative to using a multiplicative derating factor, such as K_V or K_T, when predicting timing delays through integrated circuit logic cells." Instead, Hayes teaches using "adders" to model changes in circuit performance: "The method and system of the present invention uses an additive term to model the change in performance that results when moving off the base operating condition (i.e. to an off baseline temperature and/or off baseline voltage)." (col. 5, lines 14-17).

Instead of using the multiplicative factors used and claimed by Applicants, Hayes teaches that the delay through a circuit is modeled as a function of input transition times (Tx) and output pin load capacitances (Cload) (see Figure 4 and col. 5, line 18 – col. 6, line 9). In short, Hayes does teach calculating a delay through a circuit, but does so in a manner completely different from that taught and claimed by Applicants. Namely, Hayes does not teach "providing an equation which comprises a plurality of variables and constants, wherein the plurality of constants are unknown constants and one of the variables is related to at least one of power supply voltage, distributed capacitance, distributed resistance, transistor performance, and temperature," as taught and claimed by Applicants.

The Office Action admits that Hayes does not teach changing the design of the circuit, nor does Hayes teach making the circuit. Instead, the Office Action contends that Southgate teaches these limitations. Applicants disagree.

When applying 35 U.S.C. 103, the following tenets of patent law must be adhered to:

(A) The claimed invention must be considered as a whole;

(B) The references must be considered as a whole and must suggest the desirability and thus the obviousness of making the combination;

(C) The references must be viewed without the benefit of impermissible hindsight vision afforded by the claimed invention; and

(D) Reasonable expectation of success is the standard with which obviousness is determined.

Hodosh v. Block Drug Co., Inc., 786 F.2d 1136, 1143 n.5, 229 USPQ 182, 187 n.5 (Fed. Cir. 1986).

Applicants submit that the Examiner simply has not adhered to the basic tenets of patent law as set forth by the court in *Hodosh.*

The Office Action contends that Southgate teaches a method for designing a circuit represented by blocks (citing col. 5, line 66 – col. 6, line 4; col. 6, lines 30-38) wherein a "performance analysis" is conducted, and if goals for the design have not been met, changing the first circuit design to obtain a second circuit design (citing col. 6, line 55 – col. 7, line 9; Fig. 1). As claimed, Applicants limitation is for "performing a first set of ***timing analyses*** using the performance model of the first circuit design." On the other hand, Southgate teaches that the designer creates more detailed "blocks" that describe the circuit level implementations. In other words, Southgate teaches using a "top-down" methodology to design circuits (see Summary, col. 3, lines 19-56). Southgate teaches writing the "blocks" in a file format such as VHDL or Verilog (col. 6, lines 16-21). While these Verilog or VHDL blocks describe the behavior of a block, they do not provide or generate ***timing*** information. Southgate discusses this shortcoming of the

blocks and discusses that further techniques are needed to gather and analyze timing data ***after*** the design blocks have been completely (positively) simulated (col. 6, line 55 – col 7, line 9).

This shortcoming of Southgate leads to yet another reason why the combination of Hayes in view of Southgate does not teach or suggest Applicants' claimed invention. Hayes teaches modeling of timing data using an additive approach quite different from that disclosed and claimed by Applicants, while Southgate teaches behavioral simulation using blocks of VHDL or Verilog formatted code. In combining the references, the Examiner fails to explain how timing data generated by Hayes can be used in the VHDL/Verilog code blocks taught by Southgate. Combining the timing analysis information of Hayes with the VHDL/Verilog code of Southgate shows that the Examiner did not consider Applicants' claimed invention as a whole when rejecting Applicants' claims. This is especially problematic in that Southgate teaches that its timing data is not available until ***after*** the design blocks have been completely simulated. In essence, other than the fact that both references deal with circuit design, there is absolutely no motivation to combine the references as found in the references themselves. Southgate's VHDL/Verilog blocks are completely useless to Hayes' desire to model circuit delay without using multiplicative factors. Likewise, Hayes' timing simulation that uses adders instead of multiplicative factors is useless to Southgate's use of VHDL/Verilog blocks as such timing information can only be ascertained after the VHDL/Verilog blocks are fully complete and "the entire design has been successfully simulated" (Southgate, col. 6, lines 55-58).

Applicants aver that the combination of Hayes and Southgate is improper in that it arose from the use of impermissible hindsight. As described above, Hayes focuses on a way of measuring delay using adders rather than multiplicative factors, while Southgate focuses on using blocks of VHDL/Verilog code to perform top-down circuit design. Applicants submit that these references were selected by the Examiner with the Examiner using Applicants' claimed limitations as "guideposts" for selecting the references. This assertion is made clear by the fact that the references cited by the Examiner simply do not work together. Further, neither references suggests a combination created by the Examiner. Consequently, the combination of

Hayes and Southgate shows that the Examiner used impermissible hindsight when examining and rejecting Applicants claims. Finally, Applicants note that, as explained above, that there is no reasonable expectation of success in combining the timing analysis of Hayes with the top-down VHDL/Verilog blocks of Southgate.

The rejection of claim 1 under 35 U.S.C. § 103 has been overcome. As shown above, the combination of Hayes and Southgate does not teach or suggest each limitation set forth in Applicants' claim 1. Furthermore, as described in detail above, the combination of Hayes and Southbridge is improper because it did not consider Applicants' claimed invention as a whole, the references were not considered as a whole and clearly do not suggest the desirability of making the combination, the references were viewed using impermissible hindsight, and finally, there is no reasonable expectation of success in combining the references. Claims 2-35 each depend, directly or indirectly, on claim 1 and, therefore, are allowable for at least the same reasons that claim 1 is allowable.

Applicants note that claims 13-24 were rejected under 35 U.S.C. § 103 as being obvious, and therefore unpatentable over Hayes in view of Southgate and further in view of U.S. Patent no. 6,507,935 to Aingaran et al. (hereinafter "Aingaran"). Each of these claims depends directly or indirectly on claim 1 and, therefore, are allowed for at least the same reasons that claim 1 is allowed, as set forth above. While Applicants do not agree that Aingaran teaches or suggests the claimed limitations set forth in the Office Action, Applicants aver that the base rejection of Hayes in view of Southgate of Applicants' independent claim is baseless and improper, as set forth above. Therefore discussion, at this time, of the shortcomings of Aingaran is unnecessary.

Likewise, Applicants note that claims 25-35 were rejected under 35 U.S.C. § 103 as being obvious, and therefore unpatentable over Hayes in view of Southgate and further in view of U.S. Patent no. 5,559,715 to Misheloff (hereinafter "Misheloff"). Each of these claims depends directly or indirectly on claim 1 and, therefore, are allowed for at least the same reasons that claim 1 is allowed, as set forth above. While Applicants do not agree that Misheloff teaches or suggests the claimed limitations set forth in the Office Action, Applicants aver that the base

rejection of Hayes in view of Southgate of Applicants' independent claim is baseless and improper, as set forth above. Therefore discussion, at this time, of the shortcomings of Misheloff is unnecessary.

Conclusion

Applicants respectfully submit that every rejection and objection set forth in the Office Action has been overcome. Consequently, the remaining claims are in condition for allowance and a Notice of Allowance for the remaining claims is respectfully requested. If a discussion with Applicants' attorney would be helpful in resolving any issues regarding patentability, the Examiner is invited to contact Applicants' undersigned attorney.

Respectfully submitted,

SEND CORRESPONDENCE TO:

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